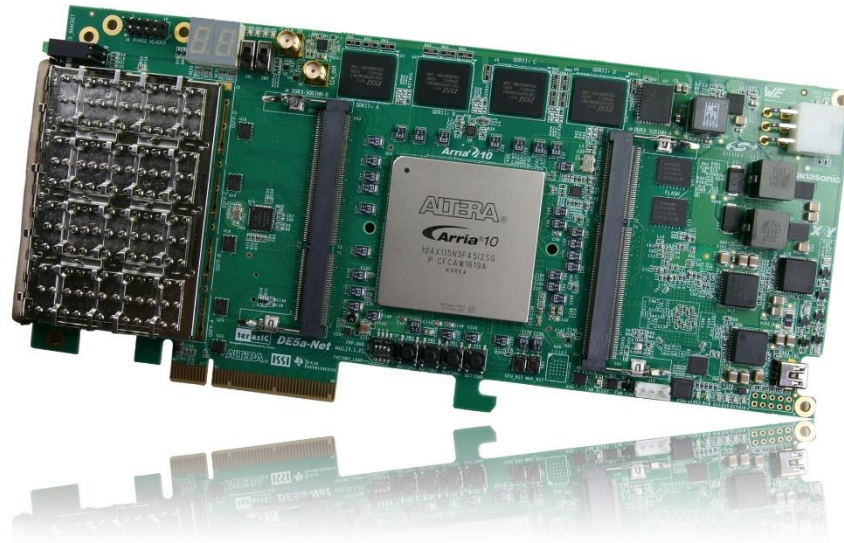


# DE5a-Net Arria 10 FPGA Development Kit

## 1. Overview



The Terasic DE5a-Net Arria 10 GX FPGA Development Kit provides the ideal hardware solution for designs that demand high capacity and bandwidth memory interfacing, ultra-low latency communication, and power efficiency. With a full-height, 3/4-length form-factor package, the DE5a-Net is designed for the most demanding high-end applications, empowered with the top-of-the-line Altera Arria 10 GX, delivering the best system-level integration and flexibility in the industry.

The Arria® 10 GX FPGA features integrated transceivers that transfer at a maximum of 12.5 Gbps, allowing the DE5a-Net to be fully compliant with version 3.0 of the PCI Express standard, as well as allowing an ultra low-latency, straight connections to four external 40G QSFP+ modules. Not relying on an external PHY will accelerate mainstream development of network applications enabling customers to deploy designs for a broad range of high-speed connectivity applications. For designs that demand high capacity and high speed for memory and storage, the DE5a-Net delivers with two independent banks of DDR3 SO-DIMM RAM, four independent banks of QDRII+ SRAM, high-speed parallel flash memory. The feature-set of the DE5a-Net fully supports all high-intensity applications such as low-latency trading, cloud computing, high-performance computing, data acquisition, network processing, and signal processing.

## 2. Specification

### FPGA

- Altera Arria 10 GX FPGA (10AX115N2F45E1SG)
- **Company: Terasic**
- **Tel: +886-3-5750880**
- **Fax: +886-3-5726690**
- **Add: 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan**

**\* FPGAs with less LEs are also available. Please contact Terasic sales team.**

## FPGA Configuration

- On-Board USB Blaster II or JTAG header for FPGA programming
- Fast passive parallel (FPPx32) configuration via MAX II CPLD and flash memory

## Memory

- 256MB FLASH
- 2 Independent DDR3 SODIMM Sockets, up to 8 GB 933 MHz or 4GB 1066MHz
- 4 Independent 550 MHz QDRII+SRAMs, 18-bits data bus and 72Mbit for each ( \* )

\* The performance of QDRII+ depends on the memory IP and the speed grade of Arria 10 device.

For E1 speed grade, the QDRII+ is capable of running at 550MHz with Altera QDRII+ IP.

For I2 speed grade, the max. frequency of QDRII+ is 467MHz.

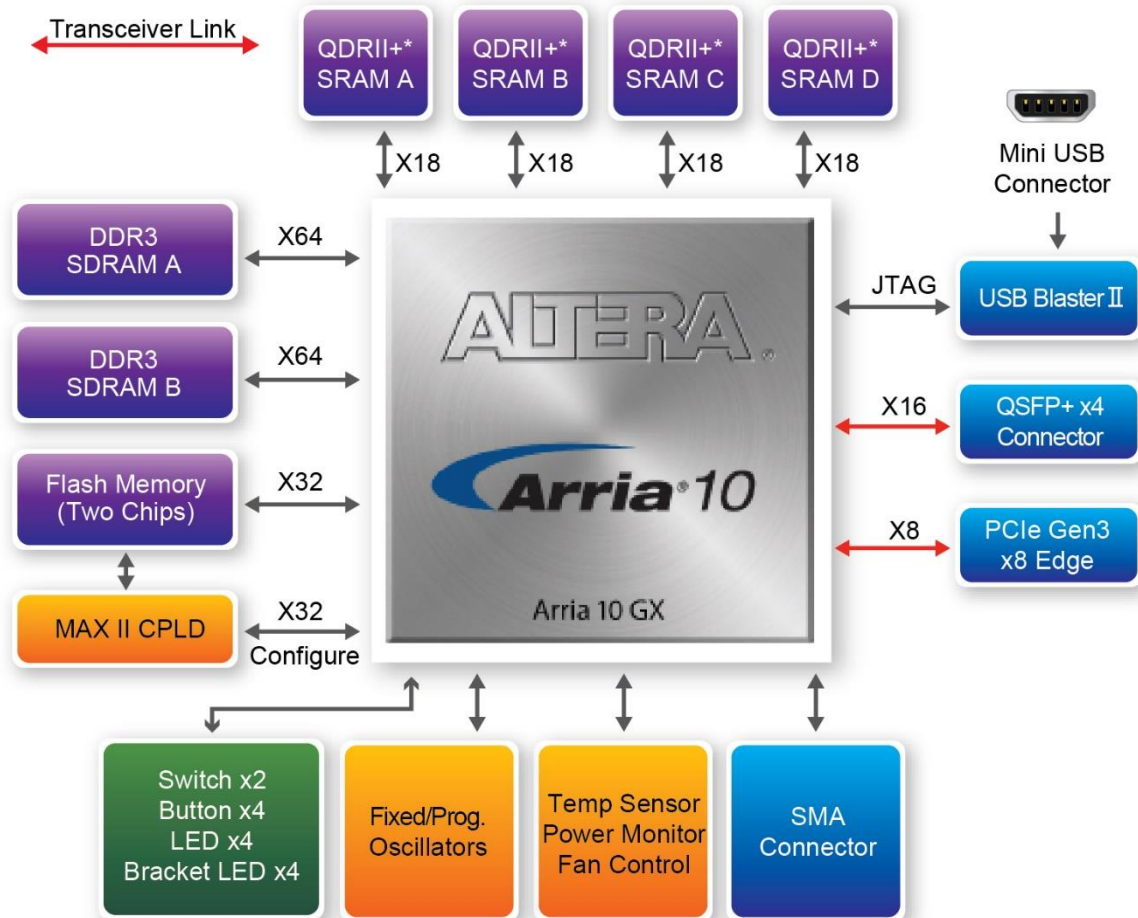
## Communication and Expansion

- Four QSFP+ connectors
- PCI Express (PCIe) x8 edge connector (includes Windows PCIe drivers)
- One RS422 expansion header

## Others

- General user input / output:
  - 2 LEDs
  - 1 Bracket LED Array
  - 4 push-buttons
  - 2 slide switches
  - SMA clock input / output
- On-Board Clock
  - 50MHz Oscillator
  - Programmable Clock Generator
- System Monitor and Control
  - Temperature sensor
  - Power Monitor
  - Fan control
- Power
  - PCI Express 6-pin power connector, 12V DC Input
  - PCI Express edge connector power
- Mechanical Specification
  - PCI Express standard height and 3/4-length
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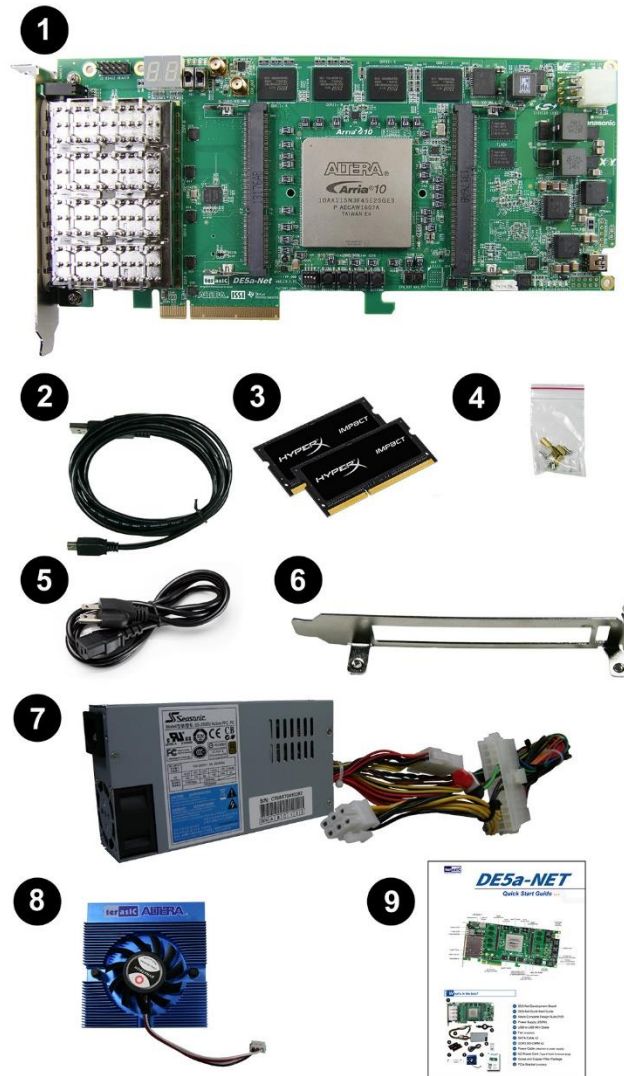
## Block Diagram



\*Cypress QDRII+ SRAM or functional compatible SRAMS provided by GSI (SigmaQuad-II+) and ISSI (QUADP).

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### 3. Kit content



1. DE5a-Net Development Board
2. USB to USB Mini Cable
3. DDR3 2133 4GB SO-DIMM x2
4. Screw & Copper Pillar Package
5. AC Power Cord (Type B North American Plug)
6. PCIe Bracket (Installed)
7. Power Supply & Power Cable
8. Fan (installed)
9. DE5a-Net Quick Start Guide

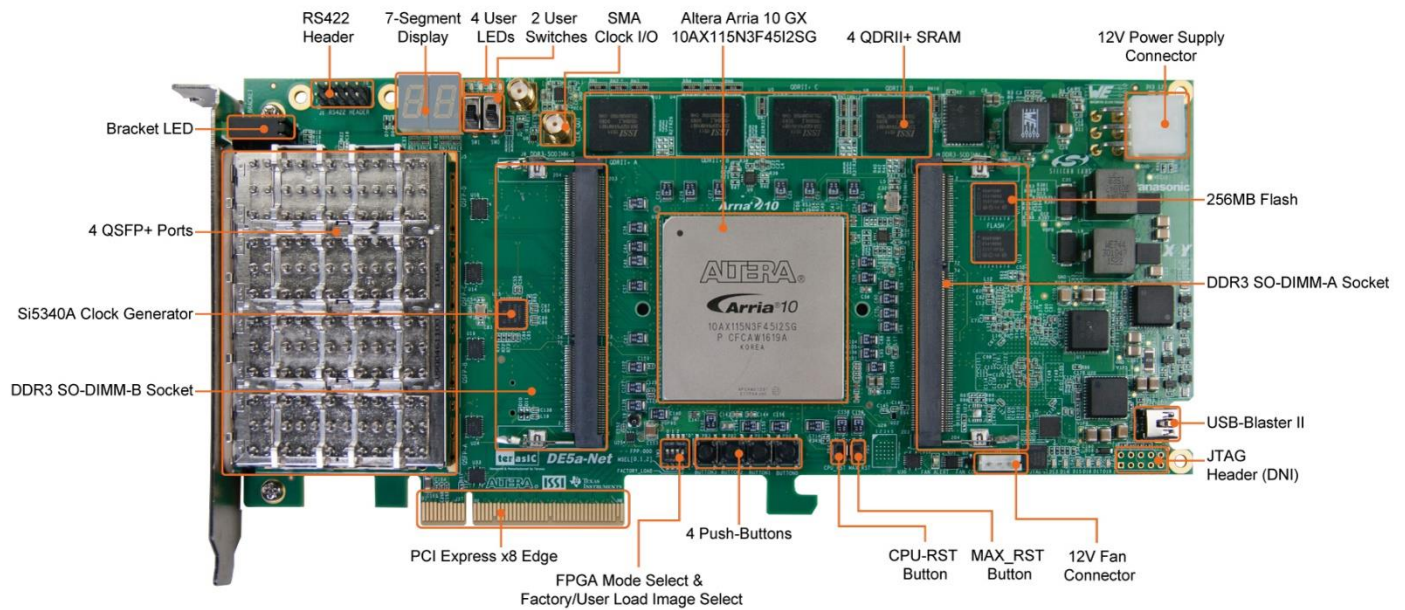
- **Quartus design software license is not included in this kit.**

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## 4. Layout

### DE5a-Net Arria 10 FPGA Development Kit



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